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| Name | Le Nhat Minh | No. |  | Div/Dept | DSD/ACD/ACT1 | Job  Date：2023/09/20  Title | Engineer |
| Please tick  the period | First Month | □W1 □W2 □W3 □W4 | | | | | |
| Second Month | □W1 □W2 □W3 🗹W4 | | | | | |
| Third Month | □W1 □W2 □W3 □W4 | | | | | |

1. The weekly report aims to help accelerate member’s workspace integration and should be reviewed by mentor on the last working day of the week.
2. The new weekly report should be reviewed and signed by mentor and direct supervisor.

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| Work Experience Record |
| 1. Please describe the tasks and achievements you learned/executed :  - Testchip: MBIST insertion |
| 2. What are the problems encountered this week? Any actions taken? Any help needed?   * Not yet |
| 3. What are the tasks for next week? Any preparation needed in advance?   * Continue with Test Chip flow |
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| Name  (Date) | Mentor | Direct Supervisor |
| Le Nhat Minh (2023/09/20) | (Signature/Date) | (Signature/Date) |

1. **Compile standard library to tessent library**

**(/home/ftv\_training/AC\_training/Intern\_Mar\_2023/Minh\_Le/FSN0FS126A/FE/DFT/MBIST/INPUT)**

* **Input file:** libcomp.do.default
* **Run file:** run\_libcomp
* **Output file:** libcomp.atpglib

1. **MBIST Insertion**

**(/home/ftv\_training/AC\_training/Intern\_Mar\_2023/Minh\_Le/FSN0FS126A/FE/DFT/MBIST/DATA\_20\_09)**

* **Input file:**FSN0FS126A.v (RD)

FSN0FS126A\_0P9V\_PLL\_src.lis (RD)

dft\_cell\_select.tcl (define cell type for MBIST insertion)

.synopsys\_dc.setup (for synthesis)

register\_tdr.dof (set static register static dft signal all\_test = 1 and MOE)

mem.list (list verilog file of memory)

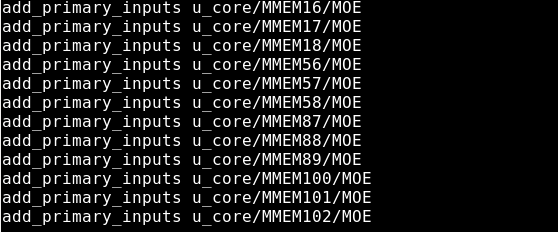
mbist\_insertion.dof (insert MBIST circuit)

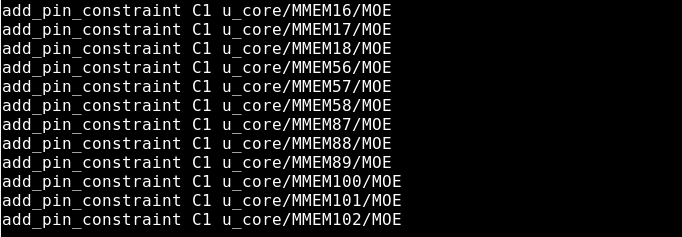
Instance\_need\_MBIST.dof (method test BIST on)

clock\_fix\_drc\_setting.dof ( add constraint for MOE pin)

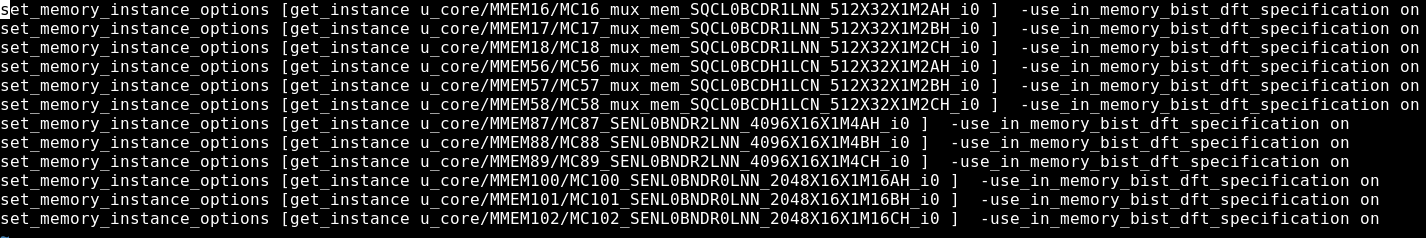
func\_debug (for synthesis)

* **Run file:** run\_mbist\_insert
* **Output file:** FSN0FS126A.vg
* **Results:**

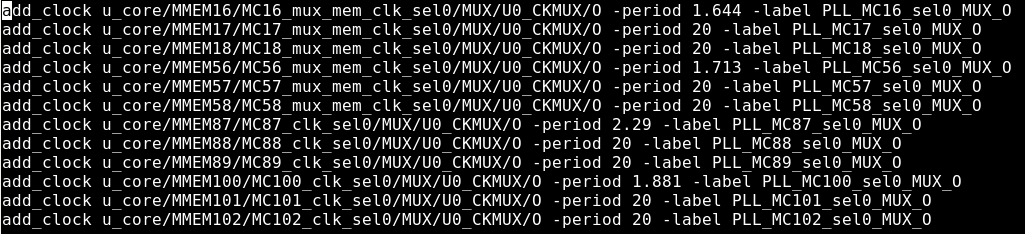
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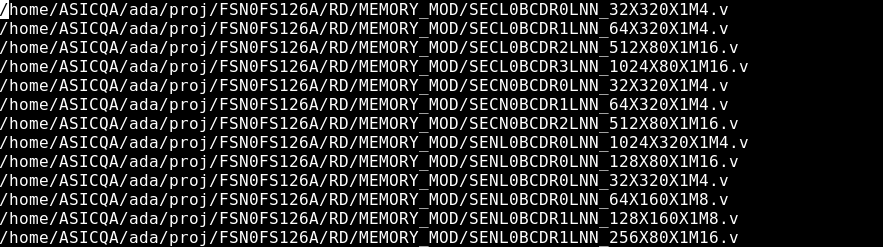
**clock\_fix\_drc\_setting**

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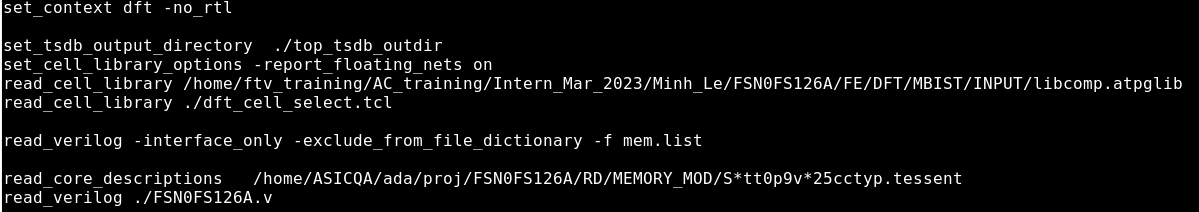
**Instance\_need\_MBIST**



**add\_clock**

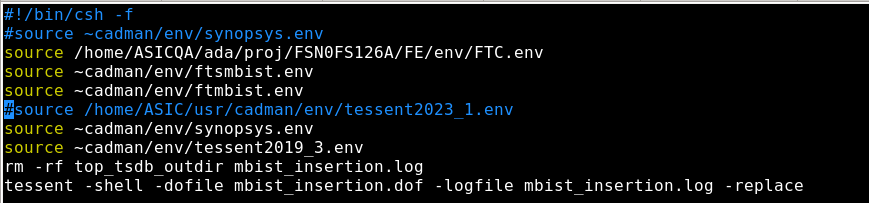
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**mem list**

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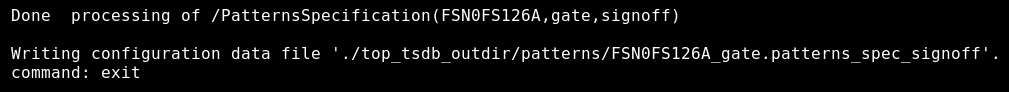
**mbist\_insertion**

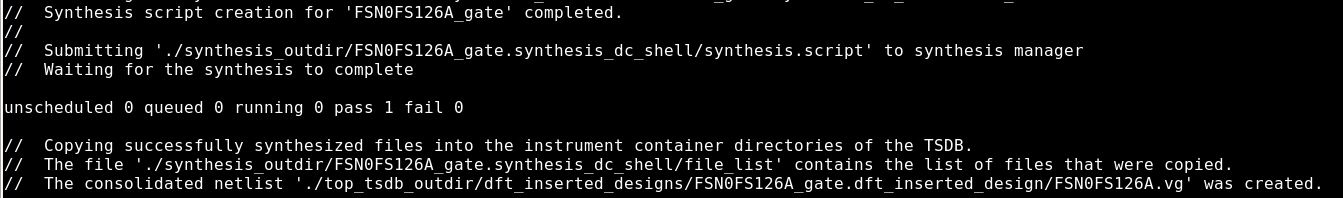
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**run\_file**

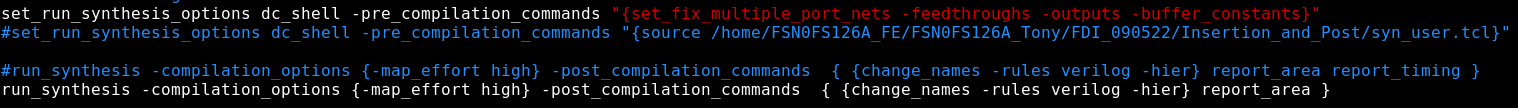
**Output:** Netlist after insert MBISTFSN0FS116A.vg

**Log file:**

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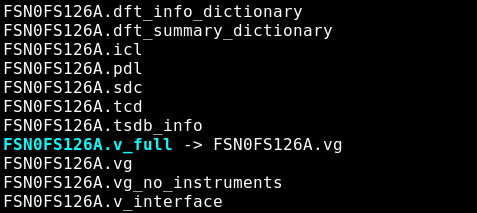
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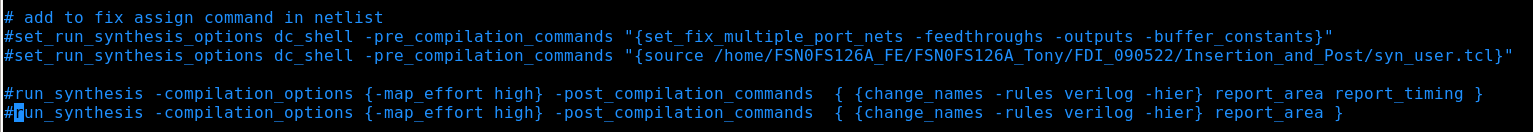
* Can’t generated file.vg if command option in file mbist\_insertion.dof



**on option**

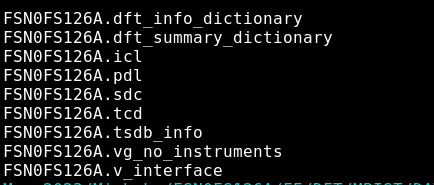
**Results:**

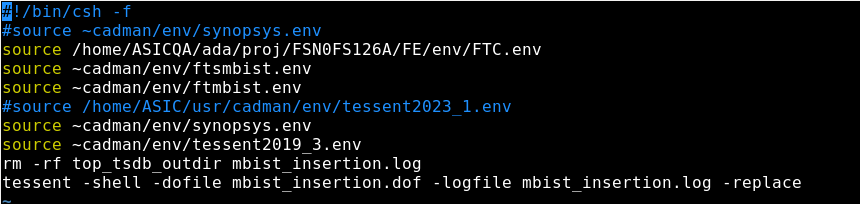
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**off option**

**Results:**

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Run file have source link project environment

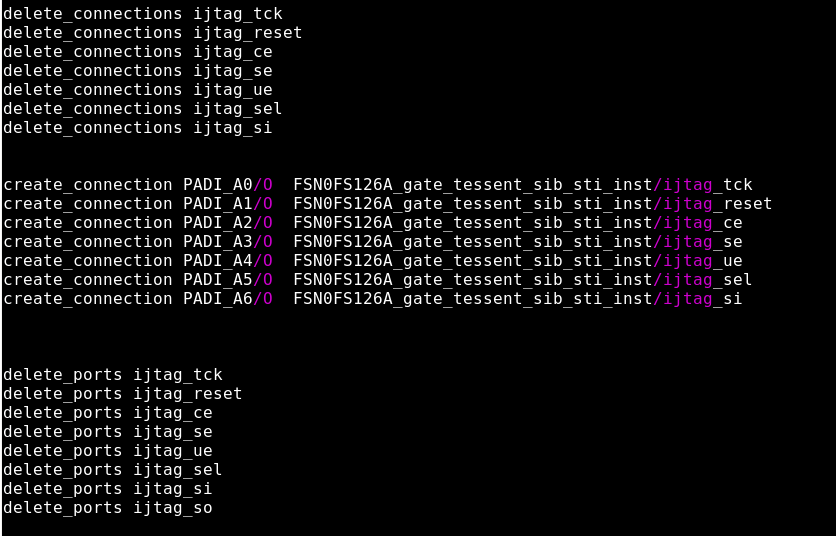
After insert MBIST circuit, perform step ts\_post.cmd (connect JTAG from module to port of chip, insert MUX to select MOE signal of memory and replace clock gatting cell by ICG)

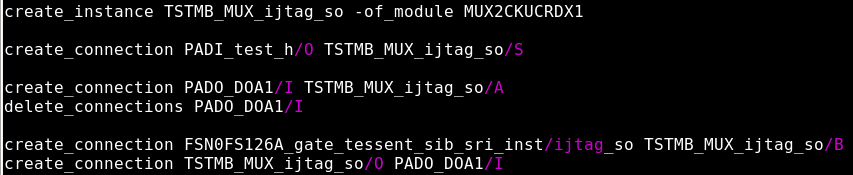
**Input files:** FSN0FS126A.vg, FSN0FS126A\_ts\_post.cmd, dft\_cell\_select.tcl, Fix\_assign.pl (connect buffer from port chip)

**Output files**: FSN0FS126A.v.tmb, FSN0FS126A.v.fixass

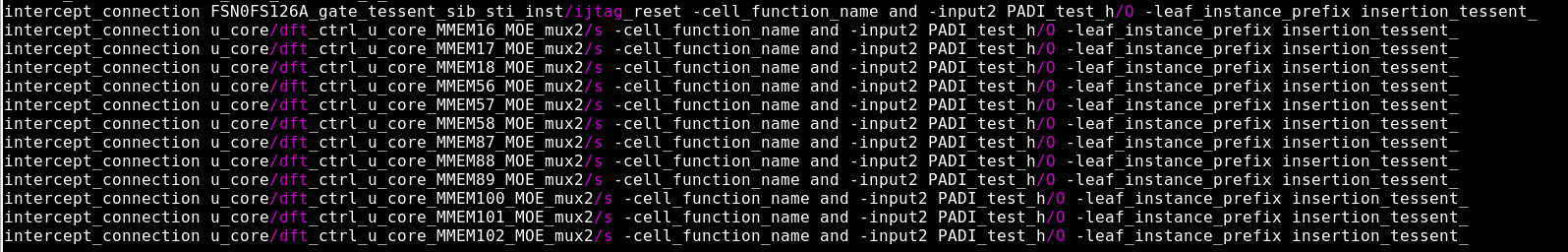
**Run files:** run\_mbist\_post.csh

Results:

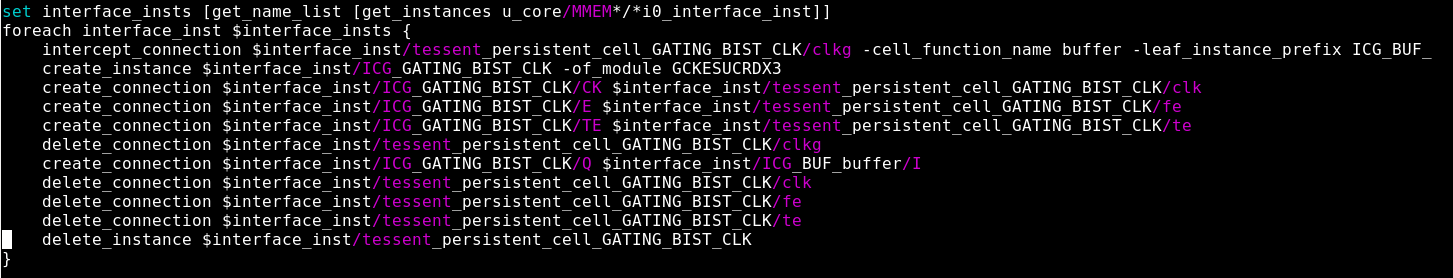




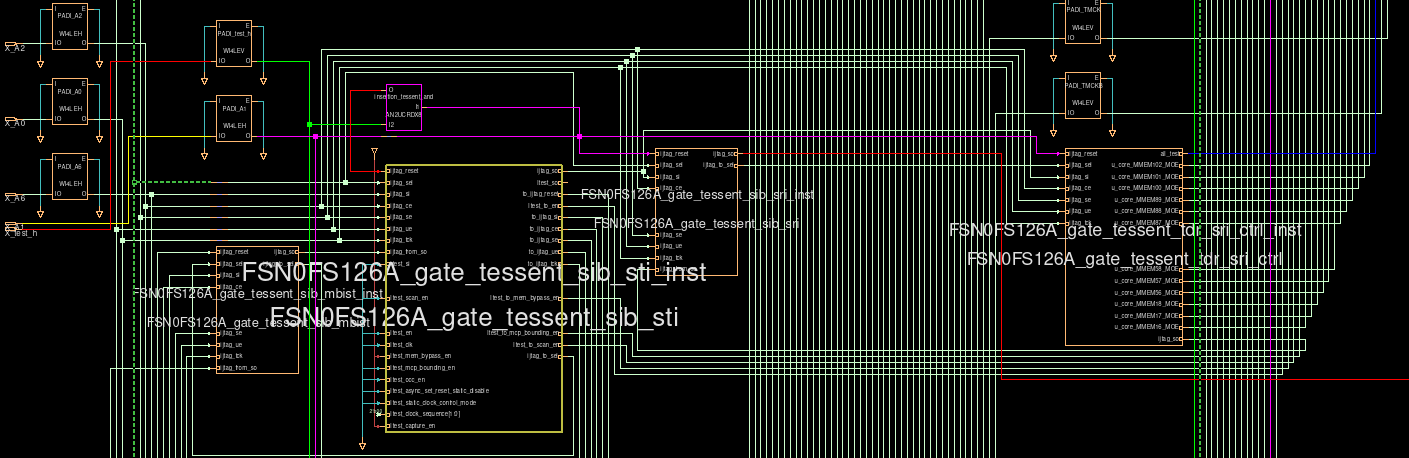
Connect JTAG pin from module to port of chip and insert MUX to control test\_mode and function mode

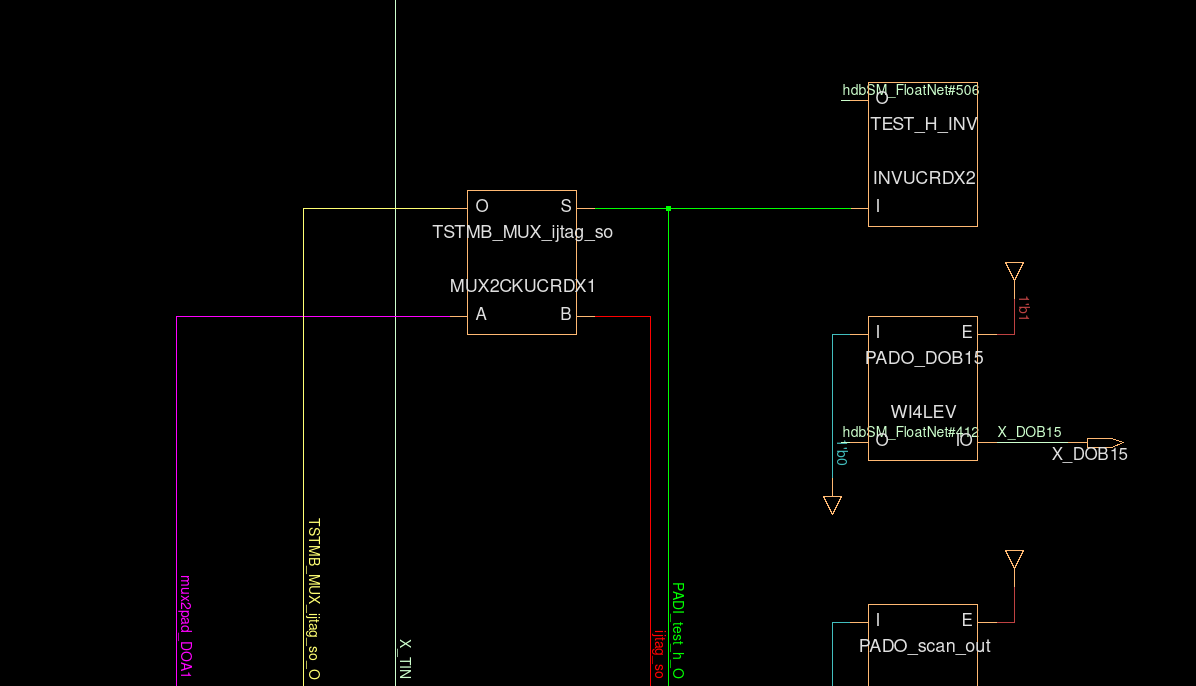


Insert AND gate (synchronized X\_A1 and X\_test\_h)

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Repalce gatting cell by ICG

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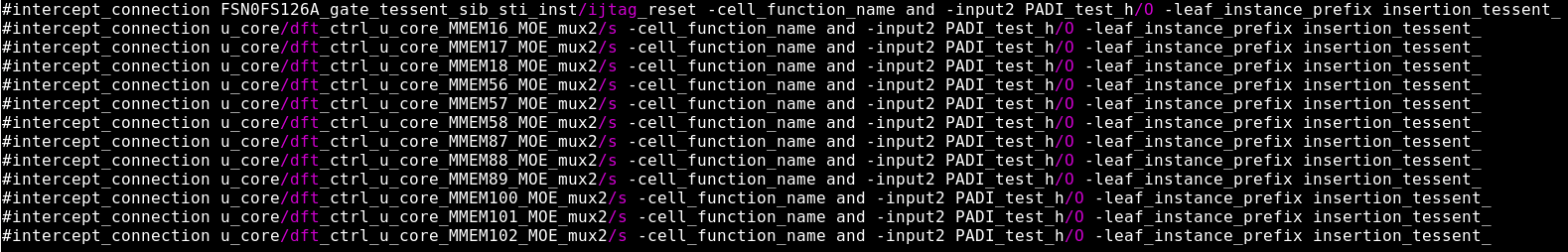
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* When X\_test\_h enable (X\_test\_h = 1) 🡺 Test\_H\_INV = 0 🡺 Test mode 🡺 Value of TSTMB\_MUX\_ijtag\_so/O = mux2pad\_DOA1.
* When X\_test\_h unenable (X\_test\_h = 0) 🡺 Test\_H\_INV = 1🡺 Function mode 🡺 Value of TSTMB\_MUX\_ijtag\_so/O = ijtag\_so

**FLEC**

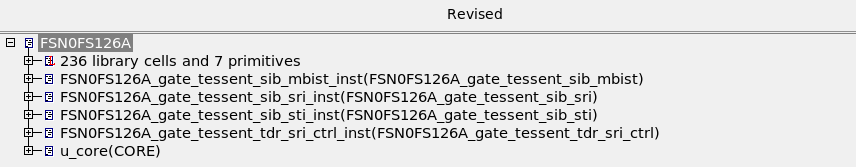
* Check with ts\_post netlist, in this case not insert AND gate

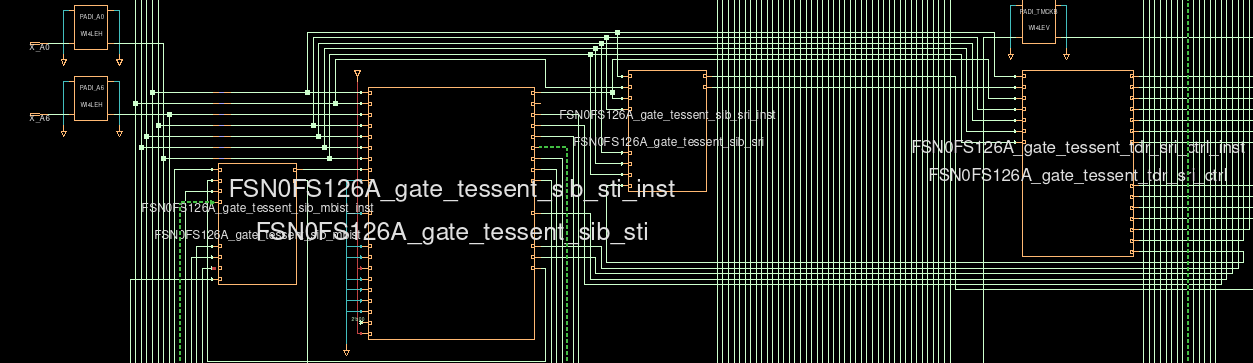
**Input file:** flec.cmd (dofile), golden netlist (RD), FSN0FS126A.v.tmb (netlist after insert MBIST)

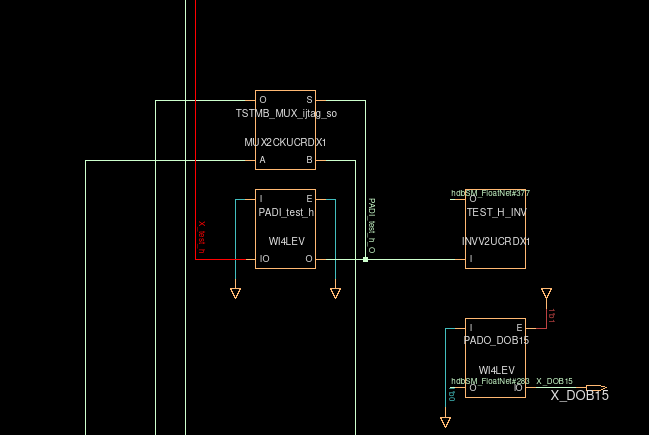


**Results:** Not equivalence



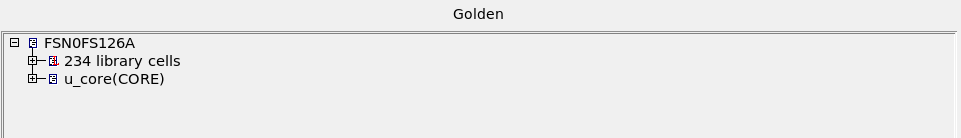


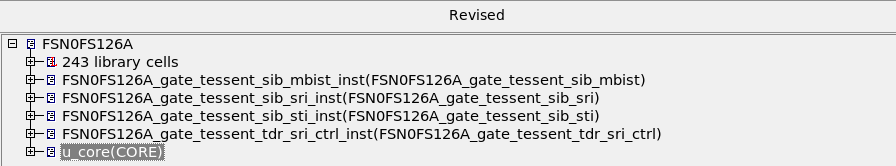


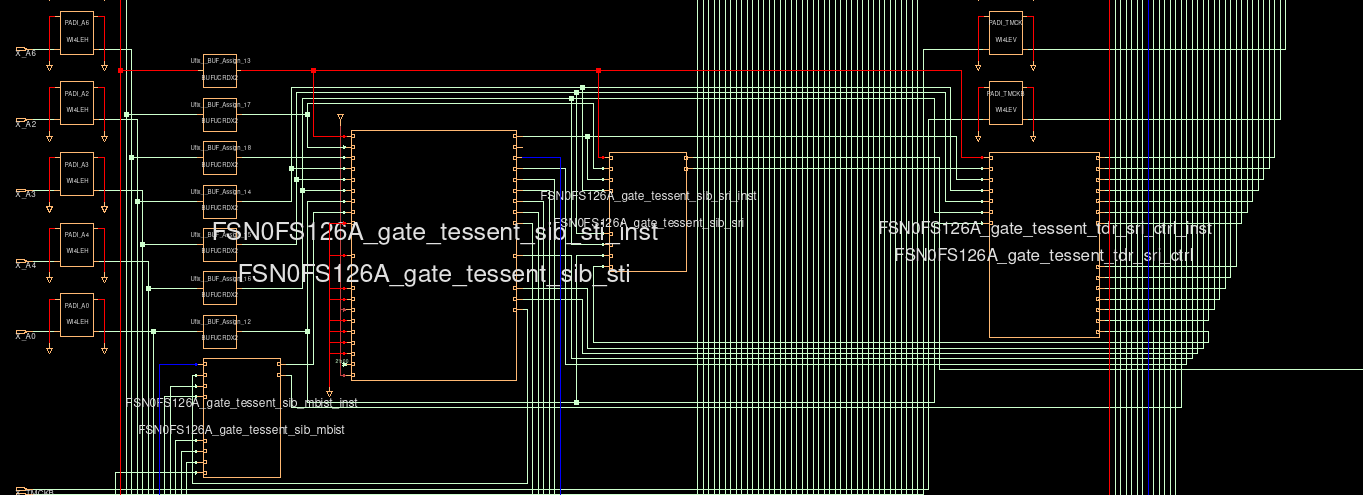


* Check with netlist fix assign (not insert AND gate)

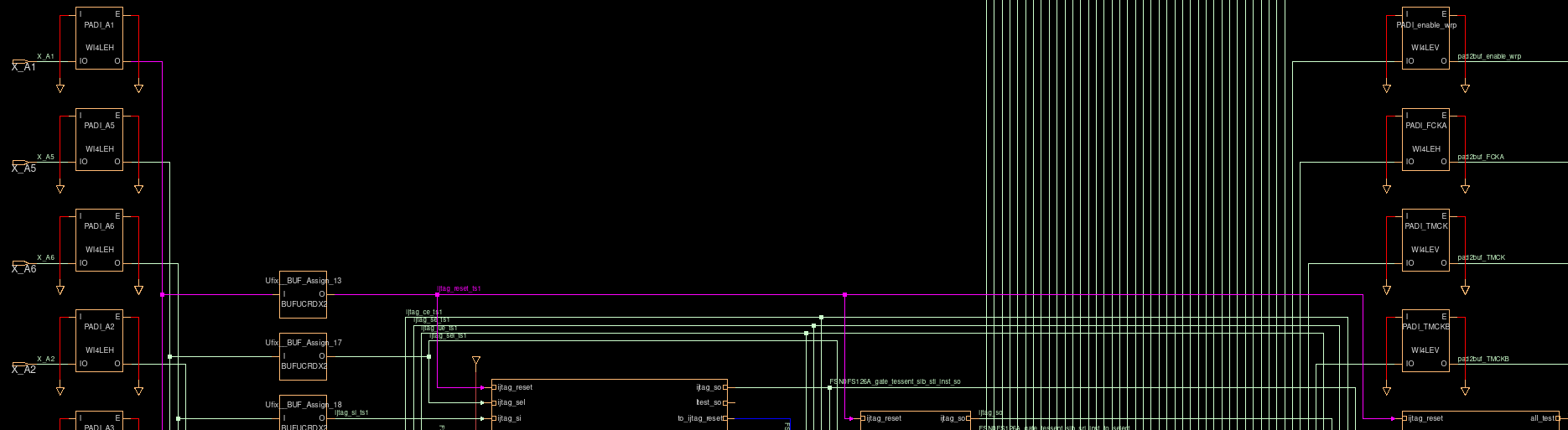
**Results:** Not equivalence

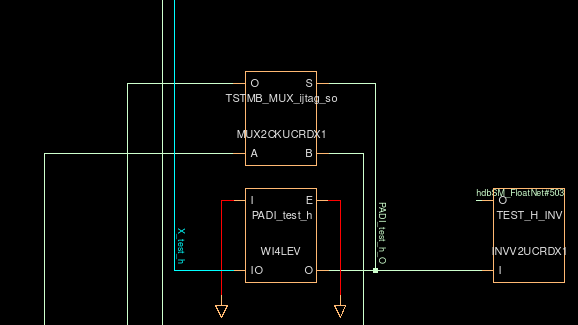






Signal IJTAG is connected with port external using buffer. However, X\_A1 direc connection with ijtag\_reset.

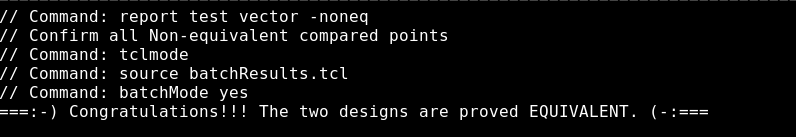




* Check with netlist after fixass

**Input file**: flec.cmd (dofile), golden netlist (RD), FSN0FS126A.v.fixass (netlist after insert MBIST), setup.ftc, gen\_no\_translate.csh

**Results**:



* Don’t need eco to fix non equivalence checking